

JEDEC STANDARD

LPDDR5/5X Compression Attached Memory Module (CAMM2) Raw Card E Annex

JESD318-F0-RCE

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Contents

	Page
1 Scope	1
2 LP5/5X CAMM2 Design File	1
3 CAMM2 Module Configuration	1
4 LP5/5X SDRAM Configuration	2
5 Supported Speeds	2
6 Design Deviations	2
7 General Layout.....	3
8 Functional Block Diagram	4
9 SMBus Net Structures.....	6
10 Host to PMIC Structures	6
11 Clock, Command/Address, Chip Select, DMI, WCK, Data, Strobe Net Structures	7
12 Compensation Lengths for Signals Per Channel	8
13 Channel Signal Net Structures.....	9
14 RESET_n Net Structure Routing.....	17
15 CAMM2 Impedance Profile	18
16 Electrically Induced Physical Damage (EIPD) Protection	19
17 Module PMIC and VR Configuration.....	20
18 SPD Programming	21
19 Cross Section Recommendations.....	22

LPDDR5/5X Compression Attached Memory Module (CAMP2) Raw Card E Annex

Contents (cont'd)

List of Tables

	Page
Table 1 — LP5/5X CAMP2 Design File	1
Table 2 — CAMP2 Module Configuration.....	1
Table 3 — LP5/5X SDRAM Configuration.....	2
Table 4 — Supported Speeds	2
Table 5 — SMBus Net Structures	6
Table 6 — Host to PMIC Structures	6
Table 7 — Compensation Lengths for Signals Per Channel.....	8
Table 8 — Channel 0A Signal Net Structure	9
Table 9 — Channel 0B Signal Net Structure.....	10
Table 10 — Channel 0C Signal Net Structure.....	11
Table 11 — Channel 0D Signal Net Structure.....	12
Table 12 — Channel 1A Signal Net Structure	13
Table 13 — Channel 1B Signal Net Structure.....	14
Table 14 — Channel 1C Signal Net Structure.....	15
Table 15 — Channel 1D Signal Net Structure.....	16
Table 16 — Trace Lengths for RESET_n Net Structure	17
Table 17 — Voltage Operating Conditions	18
Table 18 — Module PMIC and VR Configuration	20
Table 19 — SPD Programming	21
Table 20 — PCB Fabrication Table – E0.....	22

List of Figures

	Page
Figure 1 — General Layout.....	3
Figure 2 — CAMP2, Populated as Four Packages, Two Sub-Channels per Package (Part 1 of 3).....	4
Figure 3 — CAMP2, Populated as Four Packages, Two Sub-Channels per Package (Part 2 of 3).....	5
Figure 4 — CAMP2, Populated as Four Packages, Two Sub-Channels per Package (Part 3 of 3).....	6
Figure 5 — Net Structure Routing for Signals.....	7
Figure 6 — Net Structure Routing for RESET_n	17
Figure 7 — CAMP2 Impedance Profile	18
Figure 8 — Electrically Induced Physical Damage (EIPD) Protection	19
Figure 9 —Module PMIC and VR Configuration	20

LPDDR5/5X Compression Attached Memory Module (CAMM2) Raw Card E Annex

(From JEDEC Board Ballot number JCB-24-44, formulated under the cognizance of the JC-45 committee on DRAM Modules, item 2290.10).

1 Scope

This standard, JESD318-F0-RCE, "LPDDR5/5X Compression Attached Memory Module (CAMM2) Raw Card E Annex", defines the design detail of eight x16 subchannels from four 315-ball dual channel LPDDR5/5x devices. The common feature of LPDDR5/5X CAMM2, such as the connector pinout, can be found in the JESD318, DDR5/LPDDR5 Compression Attached Memory Module (CAMM2) Common Specification.

2 LP5/5X CAMM2 Design File

Table 1 — LP5/5X CAMM2 Design File

Raw Card	Applicable Design File	Applicable BOM
E0	LP5-CAMM2_RC_E0_R100_20240830.brd	LP5-CAMM2_RC_E0_R100_20240830_BOM.xlsx
NOTE 1 "Reference" design file updates will be released as needed. This CAMM2 Annex specification will reflect the most recent design files but may also be updated to reflect clarifications to the specification only. In these cases, the design files will not be updated.		

3 CAMM2 Module Configuration

Table 2 — CAMM2 Module Configuration

LPDDR5/5X SDRAM								CAMM2 Module			
Package Density (Gb)	Die Per Package	Channel Per Package	I/O Per Die	CS Per Channel	Signal Loading			Package Per CAMM2	Total LPDDR5/5X die per CAMM2	Capacity (GB)	Channel Org (Ch x I/O)
					CK C/A	CS	WCK DQ DQS				
32	2	2	16	1	1	1	1	4	8	16	8x16
64	4	2	16	2	2	1	2	4	16	32	8x16
128	8	2	8	2	4	2	2	4	32	64	8x(2x8)
256	16	2	8	4	8	2	4	4	64	128	8x(2x8)
NOTE 1 Host systems will organize into two system channels 64 I/O wide.											
NOTE 2 Product is compliant with MO-357.											

4 LP5/5X SDRAM Configuration

Table 3 — LP5/5X SDRAM Configuration

Raw Card	Supported LPDDR5/5X SDRAM Outline (Width x Length) max.(mm)	LPDDR5/5X SDRAM Package Type	Available Chip Select per Package Channel	Package Type	JEDEC MO
E0	12.5 x 15.1	315 Ball FBGA	CS[3:0]	2DP, 4DP, 8DP, 16DP	MO-338
NOTE 1 SDP is a single die per package. 2H/4H/8H denotes number of dies stacked using 3DS stacking.					

5 Supported Speeds

Table 4 — Supported Speeds

Raw Card	Speed	LPDDR5/5X-6400	LPDDR5/5X-7500	LPDDR5/5X-8533		Notes
E0	LPDDR5/5X 2DP	Y	Y	Y		1
	LPDDR5/5X 4DP	Y	Y	Y		
	LPDDR5/5X 8DP	Y	Y			
	LPDDR5/5X 16DP	Y				
NOTE 1 X reflects speed grades approved up to						
NOTE 2 Y denotes speed grade up to newly supported						

6 Design Deviations

Common Specification Length Matching for “DM, DQ and DQS within byte” and “CS and CK*” are compliant to R1.0 tolerance.

7 General Layout

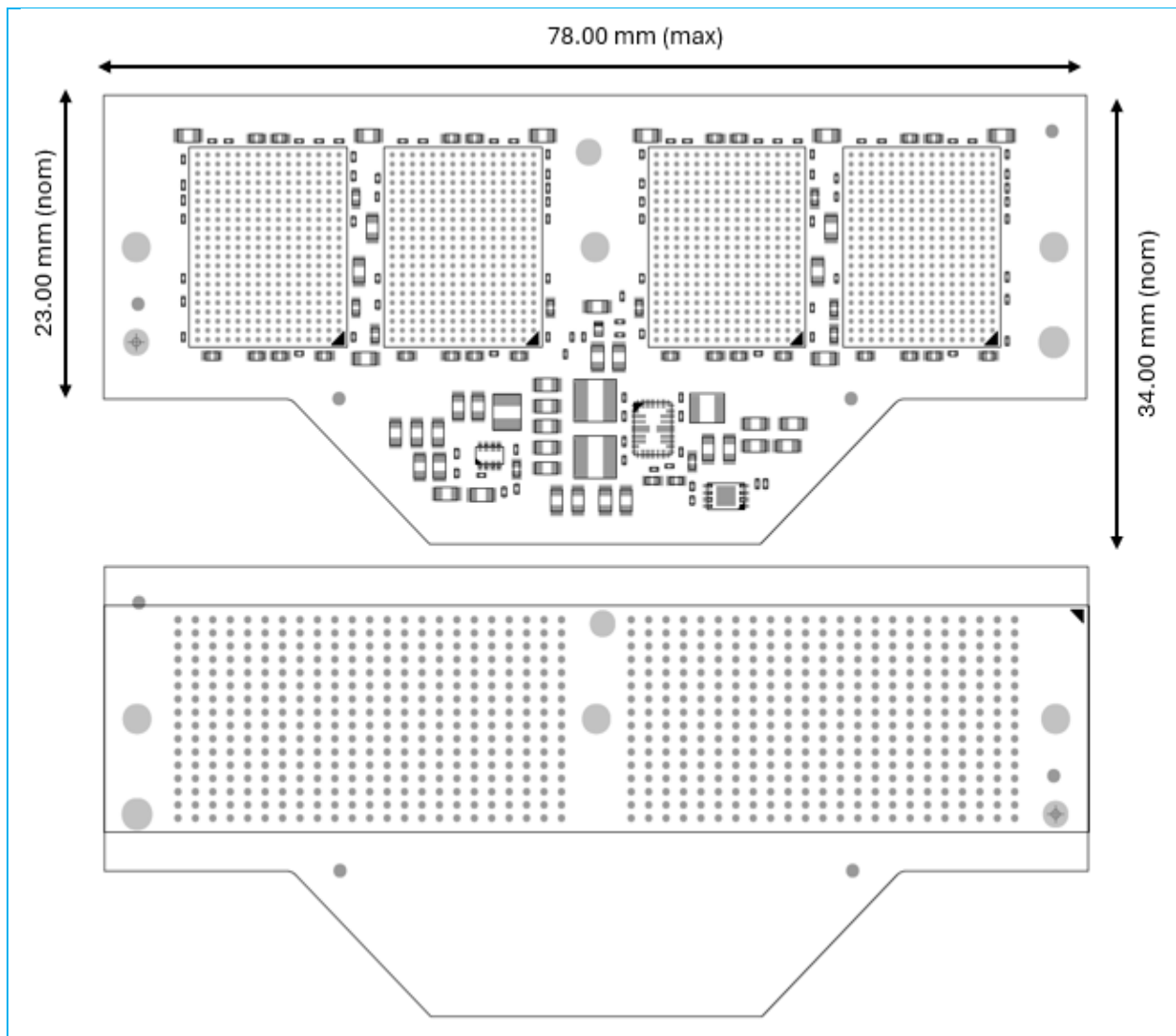


Figure 1 — General Layout

8 Functional Block Diagram

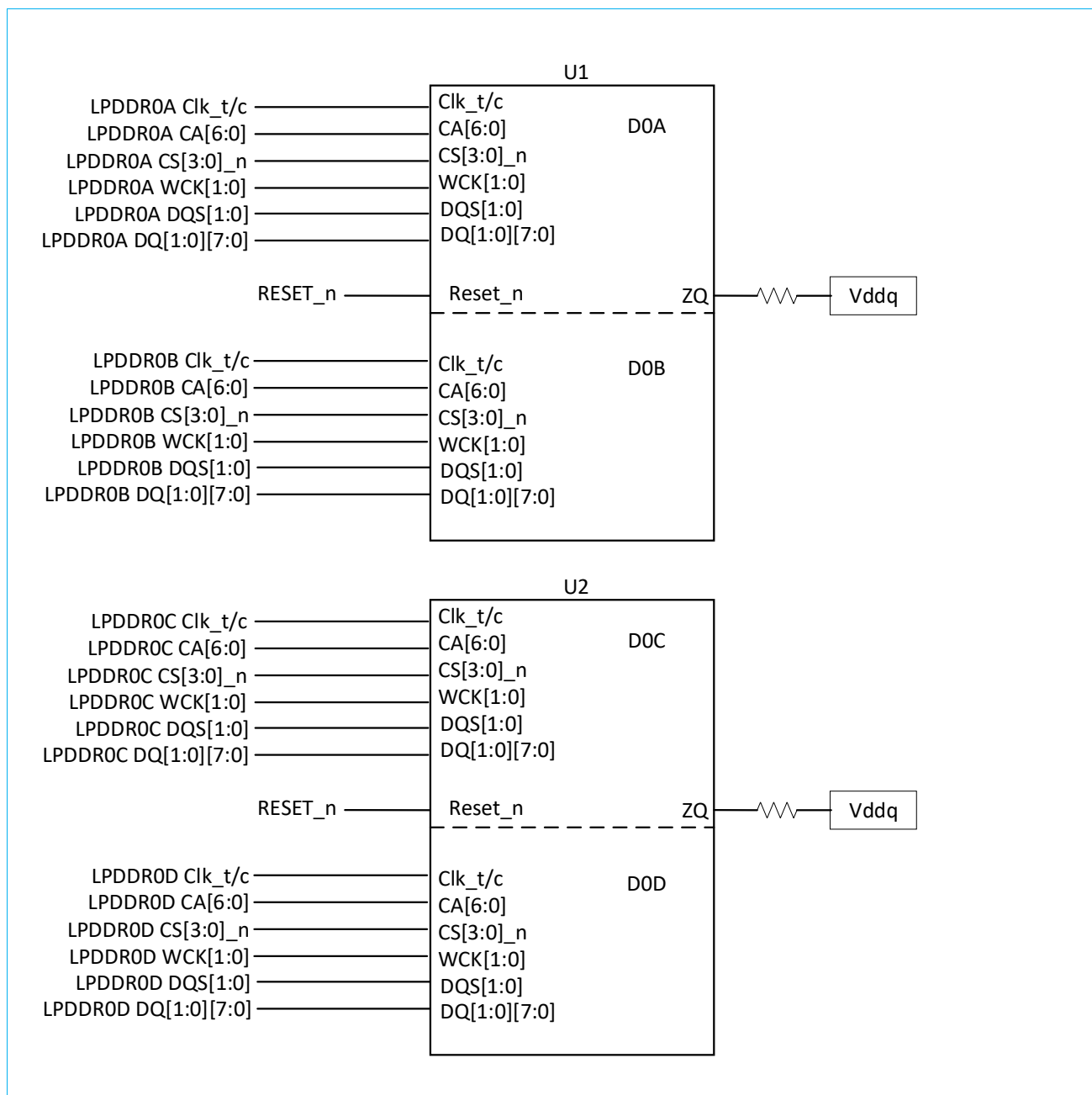


Figure 2 — CAMM2, Populated as Four Packages, Two Sub-Channels per Package (Part 1 of 3)

8 Functional Block Diagram (cont'd)

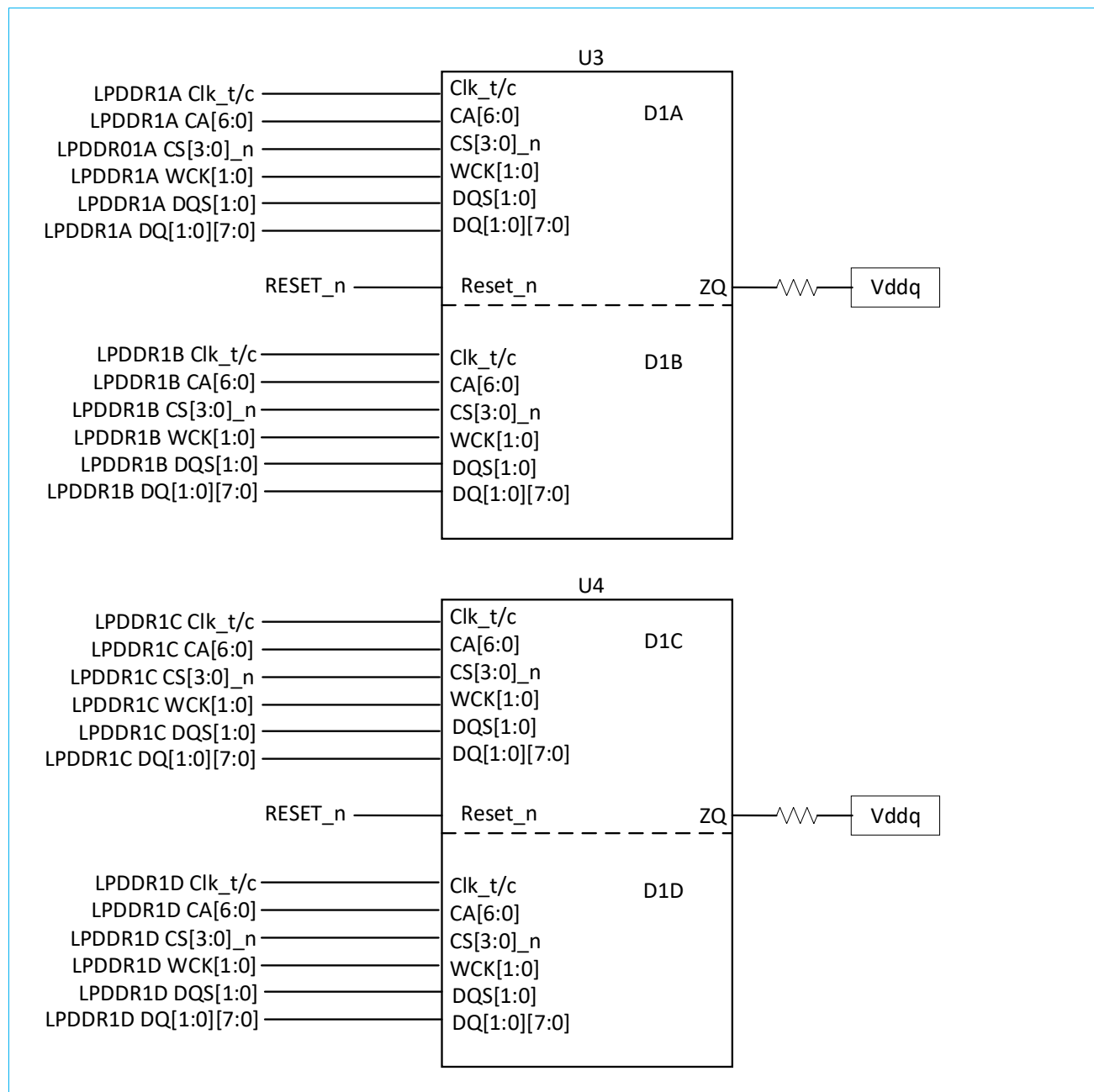


Figure 3 — CAMM2, Populated as Four Packages, Two Sub-Channels per Package (Part 2 of 3)

8 Functional Block Diagram (cont'd)

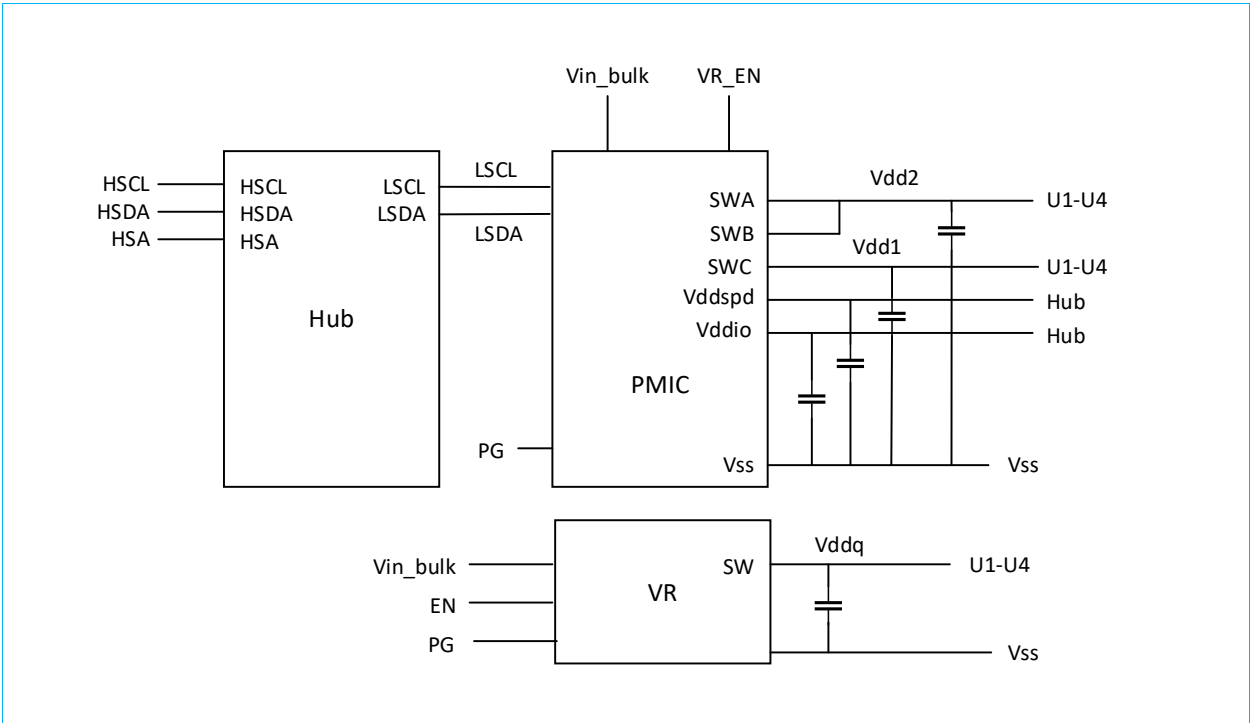


Figure 4 — CAMM2, Populated as Four Packages, Two Sub-Channels per Package (Part 3 of 3)

9 SMBus Net Structures

Table 5 — SMBus Net Structures

Signal	Etch Length (mm)		Signal	Etch Length (mm)
	CAMM2 Pin to Hub Pin			Hub to PMIC
HSCL	37.4		LSCL	10.1
HSDA	48.6		LSDA	11.2
HSA	33.0			
NOTE 1 Sideband etch length does not include via travel				

10 Host to PMIC Structures

Table 6 — Host to PMIC Structures

Signal	Etch Length (mm)
PWR_GOOD	26.7 mm
PWR_EN	51.3 mm
NOTE 1 Etch length does not include via travel.	

11 Clock, Command/Address, Chip Select, DMI, WCK, Data, Strobe Net Structures

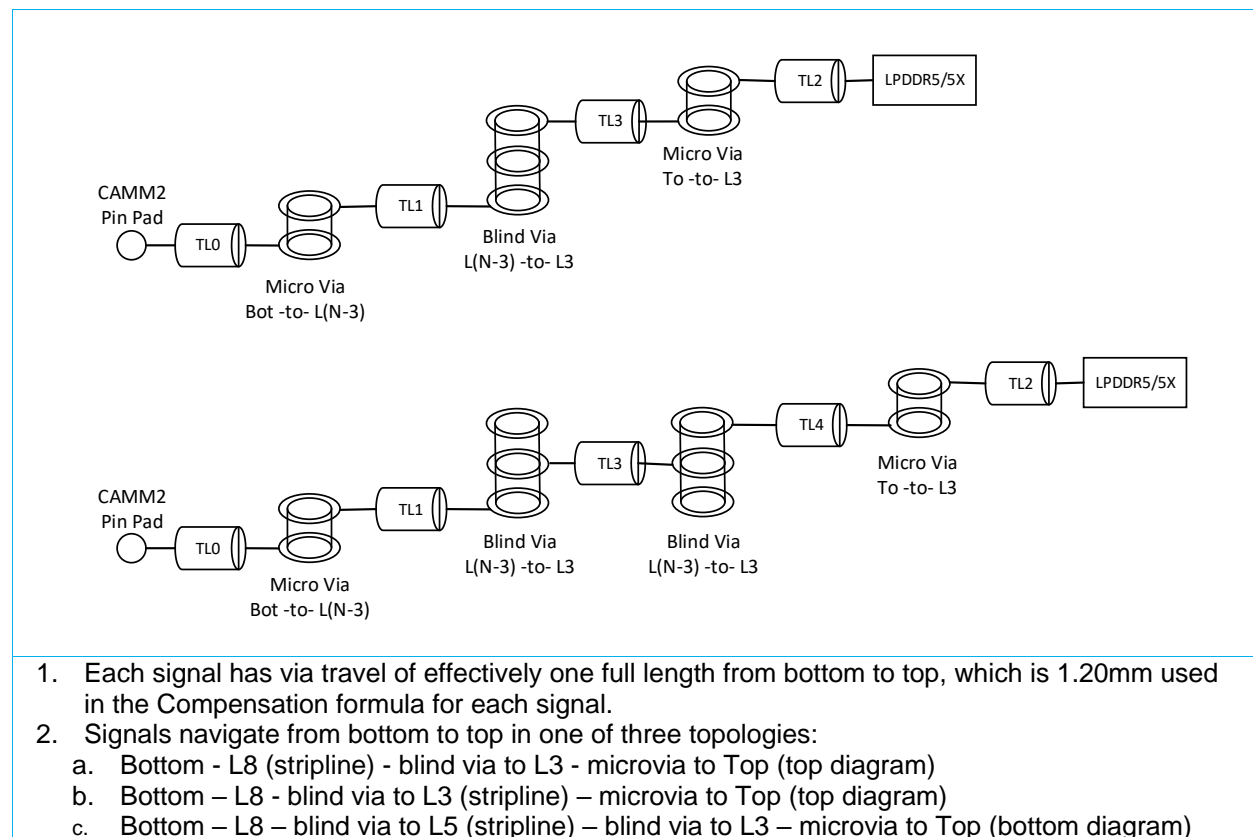


Figure 5 — Net Structure Routing for Signals

12 Compensation Lengths for Signals Per Channel

Table 7 — Compensation Lengths for Signals Per Channel

Signal	LPDDR0A	LPDDR0B	LPDDR0C	LPDDR0D	LPDDR1A	LPDDR1B	LPDDR1C	LPDDR1D
CA00	16.25	14.47	14.55	14.23	15.42	13.01	14.84	14.59
CA01	16.25	14.44	14.53	14.27	15.37	13.06	14.86	14.59
CA02	16.26	14.42	14.49	14.24	15.42	13.03	14.85	14.58
CA03	16.27	14.43	14.48	14.22	15.41	13.02	14.85	14.57
CA04	16.25	14.41	14.49	14.20	15.37	13.01	14.82	14.59
CA05	16.25	14.40	14.54	14.24	15.43	13.03	14.85	14.59
CA06	16.26	14.42	14.49	14.21	15.42	13.02	14.80	14.59
Clock_c	17.21	13.48	15.54	13.46	16.16	12.79	15.79	15.18
Clock_t	17.19	13.50	15.49	13.46	16.14	12.82	15.80	15.17
CS00_n	14.83	11.92	13.05	13.52	13.68	13.43	13.33	13.96
CS01_n	14.77	12.65	13.04	13.19	13.93	12.45	13.33	14.55
CS02_n	14.72	11.78	13.00	12.61	13.63	12.49	20.69	14.89
CS03_n	18.14	11.06	13.07	12.62	15.47	12.60	13.32	13.13
DMI0_n	14.35	13.44	12.65	13.47	14.77	13.30	12.82	13.98
DMI1_n	14.30	12.23	13.72	13.95	13.45	12.43	12.94	12.38
DQ0_0	14.39	13.44	12.66	13.47	14.81	13.27	12.86	14.02
DQ0_1	14.41	13.45	12.66	13.42	14.81	13.27	12.86	14.00
DQ0_2	14.40	13.44	12.66	13.48	14.76	13.23	12.86	14.02
DQ0_3	14.33	13.45	12.65	13.49	14.80	13.30	12.81	13.95
DQ0_4	14.40	13.43	12.67	13.42	14.81	13.29	12.87	14.01
DQ0_5	14.40	13.43	12.65	13.47	14.80	13.26	12.81	14.00
DQ0_6	14.41	13.44	12.65	13.49	14.74	13.30	12.88	13.98
DQ0_7	14.33	13.41	12.66	13.49	14.80	13.26	12.85	13.94
DQ1_0	14.34	12.22	13.72	13.91	13.52	12.43	12.93	12.36
DQ1_1	14.34	12.22	13.72	13.92	13.50	12.43	12.94	12.38
DQ1_2	14.34	12.23	13.72	13.96	13.51	12.40	12.95	12.34
DQ1_3	14.35	12.22	13.72	13.95	13.49	12.42	12.91	12.31
DQ1_4	14.35	12.22	13.72	13.95	13.46	12.42	12.90	12.36
DQ1_5	14.36	12.22	13.72	13.91	13.51	12.42	12.88	12.38
DQ1_6	14.30	12.23	13.72	13.95	13.52	12.40	12.93	12.31
DQ1_7	14.30	12.20	13.72	13.92	13.52	12.41	12.89	12.31
DQS0_c	14.55	13.16	12.26	13.28	14.28	13.70	12.78	14.44
DQS0_t	14.50	13.17	12.28	13.32	14.28	13.68	12.73	14.49
DQS1_c	13.86	12.67	14.31	13.82	14.08	12.96	12.97	12.64
DQS1_t	13.84	12.65	14.28	13.80	14.04	12.93	13.02	12.63
WCK0_c	16.24	12.56	14.51	13.44	15.34	12.59	14.80	14.30
WCK0_t	16.26	12.57	14.51	13.45	15.38	12.57	14.76	14.30
WCK1_c	16.30	12.56	14.46	13.51	15.42	12.60	14.82	14.33
WCK1_t	16.29	12.58	14.50	13.47	15.40	12.62	14.83	14.28

13 Channel Signal Net Structures

Table 8 — Channel 0A Signal Net Structure

LPDDR0A	ms	sl	sl	sl	ms			
Signal	TL0 Bot	TL1 S3	TL3 S5	TL4 S8	TL2 Top	Position Offset	Via Travel	Compensation
CA00	0.49	0.51	10.64	0.45		3	1.20	16.25
CA01	0.49	0.47	11.72	0.42		2	1.20	16.25
CA02	0.49	0.42	12.12	1.07		1	1.20	16.26
CA03	0.49	0.66	13.18	0.77		0	1.20	16.27
CA04	0.49	0.38	10.80	0.42		3	1.20	16.25
CA05	0.49	0.49	11.70	0.42		2	1.20	16.25
CA06	0.49	0.54		10.08		4	1.20	16.26
Clock_c	0.49	10.13		0.44		5	1.20	17.21
Clock_t	0.49	10.03		0.52		5	1.20	17.19
CS00_n	0.49	12.76		0.43		0	1.20	14.83
CS01_n	0.49	8.72		0.40		4	1.20	14.77
CS02_n	0.49	7.43		5.64		0	1.20	14.72
CS03_n	0.49	0.72		10.78		5	1.20	18.14
DMI0_n	0.49	0.48		7.82	0.45	4	1.20	14.35
DMI1_n	0.49	0.65		7.52	0.52	4	1.20	14.30
DQ0_0	0.49	1.26		10.49		1	1.20	14.39
DQ0_1	0.49	0.42		9.35		3	1.20	14.41
DQ0_2	0.49	0.72		12.03		0	1.20	14.40
DQ0_3	0.49	0.40		10.28		2	1.20	14.33
DQ0_4	0.49	1.16		8.59		3	1.20	14.40
DQ0_5	0.49	1.16		7.59		4	1.20	14.40
DQ0_6	0.49	10.31		0.45		2	1.20	14.41
DQ0_7	0.49	0.43		11.25		1	1.20	14.33
DQ1_0	0.49	0.72		9.97		2	1.20	14.34
DQ1_1	0.49	8.25		0.45		4	1.20	14.34
DQ1_2	0.49	11.20		0.50		1	1.20	14.34
DQ1_3	0.49	0.46		9.24		3	1.20	14.35
DQ1_4	0.49	0.68		10.02		2	1.20	14.35
DQ1_5	0.49	1.06		8.66		3	1.20	14.36
DQ1_6	0.49	10.44		0.82	0.43	1	1.20	14.30
DQ1_7	0.49	11.74		0.43	0.54	0	1.20	14.30
DQS0_c	0.49	7.18		0.73		5	1.20	14.55
DQS0_t	0.49	6.74		0.71	0.45	5	1.20	14.50
DQS1_c	0.49	0.71		6.51		5	1.20	13.86
DQS1_t	0.49	0.42		6.78		5	1.20	13.84
WCK0_c	0.49	8.14		1.05	0.45	5	1.20	16.24
WCK0_t	0.49	8.16		1.04	0.45	5	1.20	16.26
WCK1_c	0.49	8.72		0.94		5	1.20	16.30
WCK1_t	0.49	9.17		0.48		5	1.20	16.29
NOTE 1 Via travel is the same for all signals in all signal groups and is one full length from bottom to top.								
NOTE 2 Compensation Formula (TL0+TL2) / 1.1 + (TL1+TL3+TL4)+Position								

13 Channel Signal Net Structures (cont'd)

Table 9 — Channel 0B Signal Net Structure

LPDDR0B	ms	sl	sl	sl	sl			
Signal	TL0 Bot	TL1 S3	TL3 S5	TL4 S8	TL2 Top	Position Offset	Via Travel	Compensation
CA00	0.49	0.60		10.22		2	1.20	14.47
CA01	0.49	0.38	7.58	0.43	0.44	4	1.20	14.44
CA02	0.49	0.55	7.95	0.87	0.45	3	1.20	14.42
CA03	0.49	0.50	11.46	0.42	0.45	0	1.20	14.43
CA04	0.49	0.53	7.41	0.42	0.45	4	1.20	14.41
CA05	0.49	0.75	9.36	0.65		2	1.20	14.40
CA06	0.49	0.44	8.51	0.42	0.45	3	1.20	14.42
Clock_c	0.49	5.80		1.04		5	1.20	13.48
Clock_t	0.49	5.76		1.10		5	1.20	13.50
CS00_n	0.49	9.83		0.44		0	1.20	11.92
CS01_n	0.49	0.44		9.57		1	1.20	12.65
CS02_n	0.49	4.22		0.51	0.45	5	1.20	11.78
CS03_n	0.49	1.10		7.89	0.47	0	1.20	11.06
DMI0_n	0.49	0.67		11.13		0	1.20	13.44
DMI1_n	0.49	0.74		9.85		0	1.20	12.23
DQ0_0	0.49	9.37		0.42		2	1.20	13.44
DQ0_1	0.455	10.35		0.49		1	1.20	13.45
DQ0_2	0.49	7.31		0.49		4	1.20	13.44
DQ0_3	0.49	0.46		8.35		3	1.20	13.45
DQ0_4	0.49	0.85		8.93		2	1.20	13.43
DQ0_5	0.49	0.44		10.35		1	1.20	13.43
DQ0_6	0.49	1.09		7.71		3	1.20	13.44
DQ0_7	0.49	0.55		6.81	0.45	4	1.20	13.41
DQ1_0	0.49	0.62		6.96		3	1.20	12.22
DQ1_1	0.49	8.85		0.73		1	1.20	12.22
DQ1_2	0.49	0.85		5.73		4	1.20	12.23
DQ1_3	0.49	8.10		0.47		2	1.20	12.22
DQ1_4	0.49	0.68		8.89		1	1.20	12.22
DQ1_5	0.49	0.74		7.84		2	1.20	12.22
DQ1_6	0.49	7.14		0.45		3	1.20	12.23
DQ1_7	0.49	0.41		5.73	0.45	4	1.20	12.20
DQS0_c	0.49	5.96		0.56		5	1.20	13.16
DQS0_t	0.49	5.98		0.55		5	1.20	13.17
DQS1_c	0.49	5.30		0.73		5	1.20	12.67
DQS1_t	0.49	5.51		0.49		5	1.20	12.65
WCK0_c	0.49	5.24		0.67		5	1.20	12.56
WCK0_t	0.49	4.90		1.03		5	1.20	12.57
WCK1_c	0.49	5.48		0.43		5	1.20	12.56
WCK1_t	0.49	5.52		0.42		5	1.20	12.58
NOTE 1 Via travel is the same for all signals in all signal groups and is one full length from bottom to top.								
NOTE 2 Compensation Formula $(TL0+TL2) / 1.1 + (TL1+TL3+TL4)+Position$								

13 Channel Signal Net Structures (cont'd)

Table 10 — Channel 0C Signal Net Structure

LPDDR0C	ms	sl	sl	sl	sl			
Signal	TL0 Bot	TL1 S3	TL3 S5	TL4 S8	TL2 Top	Position Offset	Via Travel	Compensation
CA00	0.49	0.55	7.91	0.44		4	1.20	14.55
CA01	0.49	0.42	9.97	0.50		2	1.20	14.53
CA02	0.49	0.43	8.34	0.68	0.45	3	1.20	14.49
CA03	0.49	0.60	11.64	0.59		0	1.20	14.48
CA04	0.49	0.94	9.48	0.42		2	1.20	14.49
CA05	0.49	1.39	7.04	0.47		4	1.20	14.54
CA06	0.49	0.43	10.98	0.44		1	1.20	14.49
Clock_c	0.49	0.59		8.30		5	1.20	15.54
Clock_t	0.49	0.46		7.95	0.47	5	1.20	15.49
CS00_n	0.49	0.41	9.40	0.60		1	1.20	13.05
CS01_n	0.49	10.88		0.52		0	1.20	13.04
CS02_n	0.49	0.62		10.73		0	1.20	13.00
CS03_n	0.49	0.42	10.64	0.37		0	1.20	13.07
DMI0_n	0.49	0.65		6.35		4	1.20	12.65
DMI1_n	0.49	0.47		7.60		4	1.20	13.72
DQ0_0	0.49	0.44		8.57		2	1.20	12.66
DQ0_1	0.49	6.60		0.42		4	1.20	12.66
DQ0_2	0.49	1.00		9.02		1	1.20	12.66
DQ0_3	0.49	7.59		0.42		3	1.20	12.65
DQ0_4	0.49	8.44		0.58		2	1.20	12.67
DQ0_5	0.49	7.44		0.56		3	1.20	12.65
DQ0_6	0.49	0.43		9.57		1	1.20	12.65
DQ0_7	0.49	10.51		0.51		0	1.20	12.66
DQ1_0	0.49	10.66		0.42		1	1.20	13.72
DQ1_1	0.49	8.54		0.53		3	1.20	13.72
DQ1_2	0.49	11.18		0.89		0	1.20	13.72
DQ1_3	0.49	9.57		0.50		2	1.20	13.72
DQ1_4	0.49	0.51		7.57		4	1.20	13.72
DQ1_5	0.49	0.52		8.55		3	1.20	13.72
DQ1_6	0.49	1.06		9.02		2	1.20	13.72
DQ1_7	0.49	10.60		0.48		1	1.20	13.72
DQS0_c	0.49	4.72		0.49	0.45	5	1.20	12.26
DQS0_t	0.49	4.76		0.88		5	1.20	12.28
DQS1_c	0.49	6.97		0.70		5	1.20	14.31
DQS1_t	0.49	6.83		0.42	0.43	5	1.20	14.28
WCK0_c	0.49	0.42		7.07	0.42	5	1.20	14.51
WCK0_t	0.49	0.42		7.06	0.43	5	1.20	14.51
WCK1_c	0.49	7.15		0.66		5	1.20	14.46
WCK1_t	0.49	7.04		0.41	0.45	5	1.20	14.50
NOTE 1 Via travel is the same for all signals in all signal groups and is one full length from bottom to top.								
NOTE 2 Compensation Formula (TL0+TL2) / 1.1 + (TL1+TL3+TL4)+Position								

13 Channel Signal Net Structures (cont'd)

Table 11 — Channel 0D Signal Net Structure

LPDDR0D	ms	sl	sl	sl	sl			
Signal	TL0 Bot	TL1 S3	TL3 S5	TL4 S8	TL2 Top	Position Offset	Via Travel	Compensation
CA00	0.49	0.45	10.32	0.42	0.43	1	1.20	14.23
CA01	0.49	0.46	9.67	0.50		2	1.20	14.27
CA02	0.49	0.42	8.40	0.38	0.42	3	1.20	14.24
CA03	0.49	0.48	9.25	0.45	0.44	2	1.20	14.22
CA04	0.49	11.13		0.43		1	1.20	14.20
CA05	0.49	0.44	7.28	0.41	0.50	4	1.20	14.24
CA06	0.49	0.56	11.01	0.48	0.57	0	1.20	14.21
Clock_c	0.49	5.83		0.57	0.45	5	1.20	13.46
Clock_t	0.49	5.72		0.58	0.56	5	1.20	13.46
CS00_n	0.49	0.58		6.87	0.46	4	1.20	13.52
CS01_n	0.49	10.61		0.43	0.55	0	1.20	13.19
CS02_n	0.4666	0.48		10.51		0	1.20	12.61
CS03_n	0.49	0.53		5.45		5	1.20	12.62
DMI0_n	0.49	11.29		0.53		0	1.20	13.47
DMI1_n	0.49	11.88		0.43		0	1.20	13.95
DQ0_0	0.49	0.49		8.33		3	1.20	13.47
DQ0_1	0.49	0.52		9.69	0.63	1	1.20	13.42
DQ0_2	0.49	0.49		7.35		4	1.20	13.48
DQ0_3	0.49	0.75		9.10		2	1.20	13.49
DQ0_4	0.49	9.77		0.52	0.53	1	1.20	13.42
DQ0_5	0.49	9.30		0.53		2	1.20	13.47
DQ0_6	0.49	0.58		8.26		3	1.20	13.49
DQ0_7	0.49	0.61		7.24		4	1.20	13.49
DQ1_0	0.49	9.42		0.46	0.43	2	1.20	13.91
DQ1_1	0.49	10.46		0.43	0.42	1	1.20	13.92
DQ1_2	0.49	7.83		0.49		4	1.20	13.96
DQ1_3	0.49	0.63		8.67		3	1.20	13.95
DQ1_4	0.49	0.76		10.55		1	1.20	13.95
DQ1_5	0.49	0.49		9.22	0.61	2	1.20	13.91
DQ1_6	0.49	8.87		0.43		3	1.20	13.95
DQ1_7	0.49	7.41		0.45	0.45	4	1.20	13.92
DQS0_c	0.49	6.00		0.63		5	1.20	13.28
DQS0_t	0.49	5.47		0.80	0.45	5	1.20	13.32
DQS1_c	0.49	6.76		0.41		5	1.20	13.82
DQS1_t	0.49	6.74		0.41		5	1.20	13.80
WCK0_c	0.49	5.98		0.42	0.44	5	1.20	13.44
WCK0_t	0.49	4.94		1.42	0.50	5	1.20	13.45
WCK1_c	0.49	6.04		0.42	0.45	5	1.20	13.51
WCK1_t	0.49	6.36		0.46		5	1.20	13.47

NOTE 1 Via travel is the same for all signals in all signal groups and is one full length from bottom to top.
NOTE 2 Compensation Formula $(TL0+TL2) / 1.1 + (TL1+TL3+TL4)+Position$

13 Channel Signal Net Structures (cont'd)

Table 12 — Channel 1A Signal Net Structure

LPDDR1A	ms	sl	sl	sl	sl			
Signal	TL0 Bot	TL1 S3	TL3 S5	TL4 S8	TL2 Top	Position Offset	Via Travel	Compensation
CA00	0.49	1.24	8.84	0.69		3	1.20	15.42
CA01	0.49	0.49	10.21	0.61	0.46	2	1.20	15.37
CA02	0.49	0.85	10.98	0.95		1	1.20	15.42
CA03	0.49	0.37	12.82	0.58		0	1.20	15.41
CA04	0.49	0.40	9.87	0.46		3	1.20	15.37
CA05	0.49	0.75	10.62	0.42		2	1.20	15.43
CA06	0.49	0.87	8.32	0.58		4	1.20	15.42
Clock_c	0.49	0.59		8.52	0.45	5	1.20	16.16
Clock_t	0.49	0.87		8.21	0.45	5	1.20	16.14
CS00_n	0.49	11.62		0.42		0	1.20	13.68
CS01_n	0.49	0.53		7.76		4	1.20	13.93
CS02_n	0.49	3.84		8.14		0	1.20	13.63
CS03_n	0.49	0.46	13.01	0.37		0	1.20	15.47
DMI0_n	0.49	0.83		7.89	0.45	4	1.20	14.77
DMI1_n	0.49	0.37		7.03	0.45	4	1.20	13.45
DQ0_0	0.49	0.42		11.74		1	1.20	14.81
DQ0_1	0.49	0.83		9.33		3	1.20	14.81
DQ0_2	0.49	0.53		12.18	0.45	0	1.20	14.76
DQ0_3	0.49	10.58		0.58		2	1.20	14.80
DQ0_4	0.49	0.40		8.77		4	1.20	14.81
DQ0_5	0.49	0.41		9.74		3	1.20	14.80
DQ0_6	0.49	0.64		10.46		2	1.20	14.74
DQ0_7	0.49	11.58		0.57		1	1.20	14.80
DQ1_0	0.49	7.44		0.44		4	1.20	13.52
DQ1_1	0.49	0.49		8.37		3	1.20	13.50
DQ1_2	0.49	0.42		9.45		2	1.20	13.51
DQ1_3	0.49	10.43		0.42		1	1.20	13.49
DQ1_4	0.49	0.44		8.95	0.47	2	1.20	13.46
DQ1_5	0.49	0.45		8.42		3	1.20	13.51
DQ1_6	0.49	10.45		0.42		1	1.20	13.52
DQ1_7	0.49	11.46		0.42		0	1.20	13.52
DQS0_c	0.49	7.21		0.43		5	1.20	14.28
DQS0_t	0.49	7.22		0.41		5	1.20	14.28
DQS1_c	0.49	6.96		0.47		5	1.20	14.08
DQS1_t	0.49	6.53		0.47	0.45	5	1.20	14.04
WCK0_c	0.49	7.87		0.42	0.45	5	1.20	15.34
WCK0_t	0.49	8.25		0.49		5	1.20	15.38
WCK1_c	0.49	8.36		0.41		5	1.20	15.42
WCK1_t	0.49	8.27		0.48		5	1.20	15.40
NOTE 1 Via travel is the same for all signals in all signal groups and is one full length from bottom to top.								
NOTE 2 Compensation Formula $(TL0+TL2) / 1.1 + (TL1+TL3+TL4)+Position$								

13 Channel Signal Net Structures (cont'd)

Table 13 — Channel 1B Signal Net Structure

LPDDR1B	ms	sl	sl	sl	sl			
Signal	TL0 Bot	TL1 S3	TL3 S5	TL4 S8	TL2 Top	Position Offset	Via Travel	Compensation
CA00	0.49	0.76	8.19	0.41		2	1.20	13.01
CA01	0.49	0.62	6.28	0.51		4	1.20	13.06
CA02	0.49	0.57	6.24	1.17	0.45	3	1.20	13.03
CA03	0.49	0.62		10.32	0.47	0	1.20	13.02
CA04	0.49	0.66	6.28	0.43		4	1.20	13.01
CA05	0.49	0.41	8.00	0.57	0.45	2	1.20	13.03
CA06	0.49	0.44	8.75	0.77	0.45	1	1.20	13.02
Clock_c	0.49	5.29		0.86		5	1.20	12.79
Clock_t	0.49	5.18		0.99		5	1.20	12.82
CS00_n	0.49	10.90		0.38	0.55	0	1.20	13.43
CS01_n	0.49	0.43	8.54	0.42	0.46	1	1.20	12.45
CS02_n	0.49	0.47		5.38		5	1.20	12.49
CS03_n	0.49	0.43		10.53		0	1.20	12.60
DMI0_n	0.49	0.61		11.04		0	1.20	13.30
DMI1_n	0.49	1.31		9.47		0	1.20	12.43
DQ0_0	0.49	8.82		0.42	0.42	2	1.20	13.27
DQ0_1	0.49	0.58		9.64	0.45	1	1.20	13.27
DQ0_2	0.49	0.64		6.94		4	1.20	13.23
DQ0_3	0.49	0.49		8.17		3	1.20	13.30
DQ0_4	0.49	0.49		10.15		1	1.20	13.29
DQ0_5	0.49	0.48		9.14		2	1.20	13.26
DQ0_6	0.49	8.01		0.64		3	1.20	13.30
DQ0_7	0.49	6.64		0.54	0.47	4	1.20	13.26
DQ1_0	0.49	0.52		8.26		2	1.20	12.43
DQ1_1	0.49	9.33		0.45		1	1.20	12.43
DQ1_2	0.49	0.59		5.78	0.42	4	1.20	12.40
DQ1_3	0.49	0.54		7.23		3	1.20	12.42
DQ1_4	0.49	0.74		9.03		1	1.20	12.42
DQ1_5	0.49	8.37		0.40		2	1.20	12.42
DQ1_6	0.49	1.11		6.24	0.45	3	1.20	12.40
DQ1_7	0.49	1.18		5.13	0.50	4	1.20	12.41
DQS0_c	0.49	6.06		0.60	0.44	5	1.20	13.70
DQS0_t	0.49	6.31		0.72		5	1.20	13.68
DQS1_c	0.49	5.36		0.55	0.45	5	1.20	12.96
DQS1_t	0.49	5.80		0.49		5	1.20	12.93
WCK0_c	0.49	5.52		0.43		5	1.20	12.59
WCK0_t	0.49	5.51		0.41		5	1.20	12.57
WCK1_c	0.49	5.34		0.62		5	1.20	12.60
WCK1_t	0.49	5.42		0.55		5	1.20	12.62
NOTE 1 Via travel is the same for all signals in all signal groups and is one full length from bottom to top.								
NOTE 2 Compensation Formula (TL0+TL2) / 1.1 + (TL1+TL3+TL4)+Position								

13 Channel Signal Net Structures (cont'd)

Table 14 — Channel 1C Signal Net Structure

LPDDR1C	ms	sl	sl	sl	sl			
Signal	TL0 Bot	TL1 S3	TL3 S5	TL4 S8	TL2 Top	Position Offset	Via Travel	Compensation
CA00	0.49	0.42	8.27	0.51		4	1.20	14.84
CA01	0.49	0.51	10.29	0.42		2	1.20	14.86
CA02	0.49	0.96	8.06	1.18		3	1.20	14.85
CA03	0.49	0.48	12.18	0.54		0	1.20	14.85
CA04	0.49	0.51	8.85	1.41	0.45	2	1.20	14.82
CA05	0.49	0.62	8.17	0.41		4	1.20	14.85
CA06	0.49	0.38	10.86	0.44	0.53	1	1.20	14.80
Clock_c	0.49	8.73		0.41		5	1.20	15.79
Clock_t	0.49	8.73		0.43		5	1.20	15.80
CS00_n	0.49	0.38		10.30		1	1.20	13.33
CS01_n	0.49	11.25		0.43		0	1.20	13.33
CS02_n	0.49	0.66		13.39		5	1.20	20.69
CS03_n	0.49	0.37		11.30		0	1.20	13.32
DMI0_n	0.49	0.46		6.17	0.60	4	1.20	12.82
DMI1_n	0.49	6.87		0.43		4	1.20	12.94
DQ0_0	0.49	0.43		8.79		2	1.20	12.86
DQ0_1	0.49	6.80		0.42		4	1.20	12.86
DQ0_2	0.49	0.44		9.77		1	1.20	12.86
DQ0_3	0.49	0.62		7.54		3	1.20	12.81
DQ0_4	0.49	0.60		8.62		2	1.20	12.87
DQ0_5	0.49	0.93		7.24		3	1.20	12.81
DQ0_6	0.49	9.75		0.48		1	1.20	12.88
DQ0_7	0.49	10.03		1.18		0	1.20	12.85
DQ1_0	0.49	0.41		9.88		1	1.20	12.93
DQ1_1	0.49	0.52		7.78		3	1.20	12.94
DQ1_2	0.49	0.40		10.91		0	1.20	12.95
DQ1_3	0.49	0.43		8.42	0.45	2	1.20	12.91
DQ1_4	0.49	0.94		5.89	0.47	4	1.20	12.90
DQ1_5	0.49	0.74		7.02	0.52	3	1.20	12.88
DQ1_6	0.49	8.87		0.42		2	1.20	12.93
DQ1_7	0.49	0.44		9.41	0.45	1	1.20	12.89
DQS0_c	0.49	0.59		5.14	0.45	5	1.20	12.78
DQS0_t	0.49	0.38		5.70		5	1.20	12.73
DQS1_c	0.49	0.51		5.81		5	1.20	12.97
DQS1_t	0.49	0.42		5.96		5	1.20	13.02
WCK0_c	0.49	6.97		0.78	0.45	5	1.20	14.80
WCK0_t	0.49	7.63		0.48		5	1.20	14.76
WCK1_c	0.49	7.35		0.42	0.45	5	1.20	14.82
WCK1_t	0.49	6.82		0.96	0.45	5	1.20	14.83
NOTE 1 Via travel is the same for all signals in all signal groups and is one full length from bottom to top.								
NOTE 2 Compensation Formula $(TL0+TL2) / 1.1 + (TL1+TL3+TL4)+Position$								

13 Channel Signal Net Structures (cont'd)

Table 15 — Channel 1D Signal Net Structure

LPDDR1D	ms	sl	sl	sl	sl			
Signal	TL0 Bot	TL1 S3	TL3 S5	TL4 S8	TL2 Top	Position Offset	Via Travel	Compensation
CA00	0.49	0.41	9.11	0.42		3	1.20	14.59
CA01	0.49	0.47	10.05	0.42		2	1.20	14.59
CA02	0.49	0.88	8.64	0.42		3	1.20	14.58
CA03	0.49	0.62	9.92	0.39		2	1.20	14.57
CA04	0.49	0.57	10.95	0.42		1	1.20	14.59
CA05	0.49	0.41	8.08	0.46		4	1.20	14.59
CA06	0.49	0.44	12.05	0.45		0	1.20	14.59
Clock_c	0.49	0.52		8.01		5	1.20	15.18
Clock_t	0.49	0.70		7.83		5	1.20	15.17
CS00_n	0.49	7.49		0.42	0.44	4	1.20	13.96
CS01_n	0.49	11.96		0.42	0.58	0	1.20	14.55
CS02_n	0.49	12.32		0.38	0.60	0	1.20	14.89
CS03_n	0.49	6.07		0.42		5	1.20	13.13
DMI0_n	0.49	0.38		11.57	0.43	0	1.20	13.98
DMI1_n	0.49	0.57		10.16		0	1.20	12.38
DQ0_0	0.49	8.93		0.45		3	1.20	14.02
DQ0_1	0.49	0.48		10.88		1	1.20	14.00
DQ0_2	0.49	7.96		0.42		4	1.20	14.02
DQ0_3	0.49	0.61		9.70		2	1.20	13.95
DQ0_4	0.49	0.42		10.95		1	1.20	14.01
DQ0_5	0.49	0.59		9.76		2	1.20	14.00
DQ0_6	0.49	0.78		8.17	0.42	3	1.20	13.98
DQ0_7	0.49	0.39		7.90		4	1.20	13.94
DQ1_0	0.49	0.45		8.27		2	1.20	12.36
DQ1_1	0.49	0.44		9.29		1	1.20	12.38
DQ1_2	0.49	5.86		0.42	0.45	4	1.20	12.34
DQ1_3	0.49	0.43		6.83	0.45	3	1.20	12.31
DQ1_4	0.49	1.20		8.52		1	1.20	12.36
DQ1_5	0.49	0.41		8.32		2	1.20	12.38
DQ1_6	0.49	7.17		0.49		3	1.20	12.31
DQ1_7	0.49	5.80		0.41	0.50	4	1.20	12.31
DQS0_c	0.49	0.54		7.26		5	1.20	14.44
DQS0_t	0.49	0.66		7.18		5	1.20	14.49
DQS1_c	0.49	5.58		0.42		5	1.20	12.64
DQS1_t	0.49	5.55		0.43		5	1.20	12.63
WCK0_c	0.49	7.24		0.42		5	1.20	14.30
WCK0_t	0.49	7.24		0.42		5	1.20	14.30
WCK1_c	0.49	0.78		6.90		5	1.20	14.33
WCK1_t	0.49	0.83		6.42	0.43	5	1.20	14.28
NOTE 1 Via travel is the same for all signals in all signal groups and is one full length from bottom to top.								
NOTE 2 Compensation Formula $(TL0+TL2) / 1.1 + (TL1+TL3+TL4)+Position$								

14 RESET_n Net Structure Routing

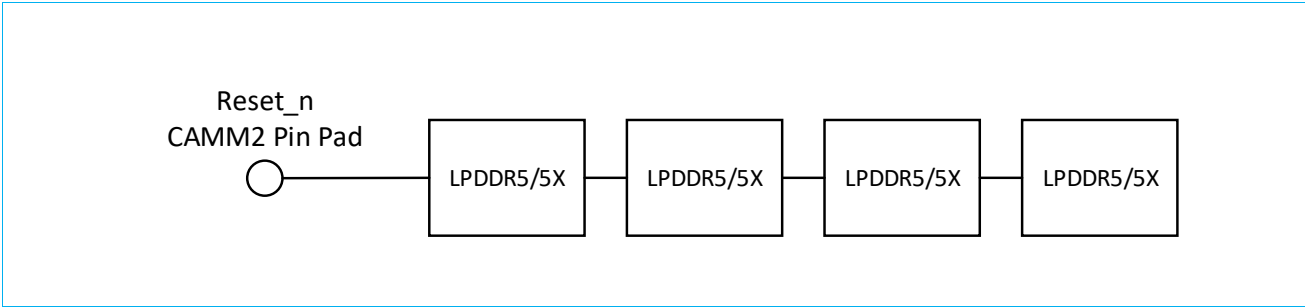


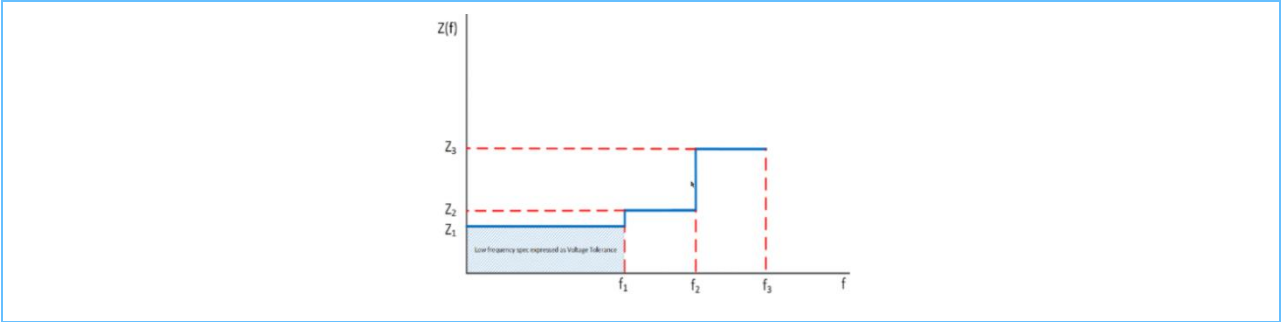
Figure 6 — Net Structure Routing for RESET_n

Table 16 — Trace Lengths for RESET_n Net Structure

Raw Card	Signal	Total Net Length (mm)	Notes
E0	RESET_n	134.3	
NOTE 1 RESET_n is total etch length. This length is for reference and not required to be met.			

15 CAMM2 Impedance Profile

Applies to VDD, VDDQ, and VPP voltage rails for this raw card.
Frequency ranges f1, f2, f3 are defined as: f1 ≤ 2 MHz; f2 = 10 MHz; f3 = 20 MHz



- NOTE 1 Z(f) targets for each frequency range (Z1, Z2, Z3).
NOTE 2 Z_x is expressed as voltage tolerance based on LPDDR5 input supply tolerances.

Figure 7 — CAMM2 Impedance Profile

Table 17 — Voltage Operating Conditions

Raw Card	LPDDR5/5X SDRAM	Symbol	Voltage Spec				Z(f) Spec	
							2 to 10 MHz	10 to 20 MHz
			Minimum	Typical	Maximum	Unit	Z _{max} (mOhm)	Z _{max} (mOhm)
E0	Core Power	VDD2H	1.01	1.05	1.12	V	5	5.5
		VDD2L	1.01	1.05	1.12		5	5.5
	Supply voltage	VDDQ ⁵	0.47	0.5	0.57	V	2.5	4
	Supply Voltage	VDD1	1.7	1.8	1.95	V	15	30
<p>NOTE 1 Power up and Power down sequencing to follow LPDDR5/5X device specification requirements.</p> <p>NOTE 2 DC to 2 MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations.</p> <p>NOTE 3 Z(f) is per voltage domain per LPDDR5/5X SDRAM device. Per device BGA pin is not required.</p> <p>NOTE 4 Z(f) does not include the LPDDR5/5X SDRAM package and silicon die.</p> <p>NOTE 5 RC-E0 does not have capability to switch between Vddq 0.5 V and 0.3 V.</p> <p>NOTE 6 RC-E0 VDD2H and VDD2L rails are tied together.</p>								

16 Electrically Induced Physical Damage (EIPD) Protection

Protection is provided to the Vin_bulk rail with a discrete Transient Voltage Suppressor (TVS).

The Vin_bulk rail TVS will be an 0402 (1006 metric) footprint in artwork. The TVS for this raw card is placed between the CAMM2 Vin_bulk pins and the PMIC. The CAMM2 supplier selects if the TVS is to be uni-directional or bi-directional. The TVS electrical characteristics to be determined by the CAMM2 supplier. V_{rw} nominal voltage of 6 V. V_{clamp} is to be less than or equal to the EOS requirement level contained in the PMIC specification.

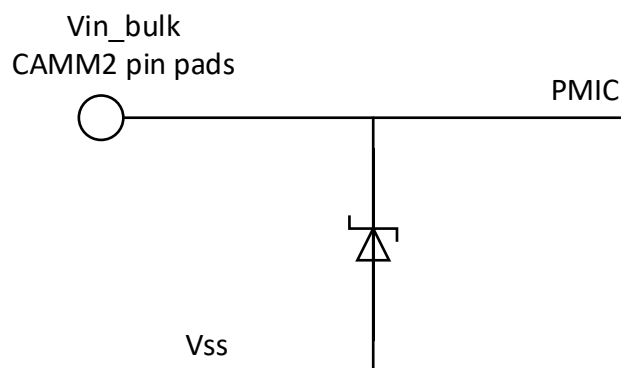


Figure 8 — Electrically Induced Physical Damage (EIPD) Protection

See Raw Card E0 registration for placement.

17 Module PMIC and VR Configuration

Define the operating mode, component type, and values for module PMIC/VR.

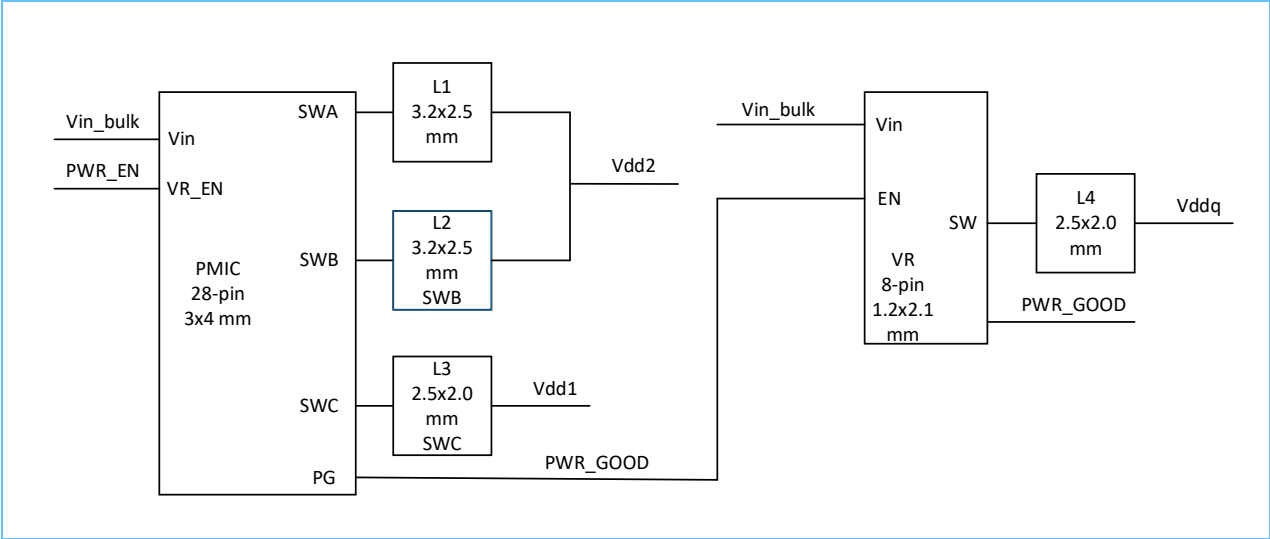


Figure 9 —Module PMIC and VR Configuration

Table 18 — Module PMIC and VR Configuration

PMIC		VDD2 (Dual Phase)		VDD1	Vddq	Notes
		SWA	SWB	SWC		
5100	SW Frequency [kHz] ²	500 (alt) 750	500 (alt) 750	500 750 (alt)		
	Inductor [μH]	0.68 ¹ 0.47 ¹	0.68 ¹ 0.47 ¹	1.0 ¹		
VR	SW Frequency [MHz] ¹				2.0	
	Inductor [μH]				0.220	3
NOTE 1 CAMM2 vendor selects inductor and SW frequency to optimize product.						
NOTE 2 28-pin PMIC for RC-E0 is operated in dual phase mode only.						
NOTE 3 VR mode is selected by the CAMM2 supplier with resistor placement. Normal operation is power save mode.						
NOTE 4 PMIC power up, power down and soft stop to follow PMIC specification.						

18 SPD Programming

Table 19 — SPD Programming

SPD	Byte	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
E0	2	0	0	0	1	0	0	1	1	0x13	LPDDR5
	2	0	0	0	1	0	1	0	1	0x15	LPDDR5X
	3	0	0	0	0	1	0	0	0	0x08	CAMM2
	6	1	0	0	1	0	1	0	1	0x95	2DP
		1	0	1	1	0	1			0xB5	4DP
		1	1	1	1	1	0			0xF9	8DP
		1	1	1	0	1	0			0xE9	16DP
	12	0	0	0	0	0	0	1	0	0x02	2DP
			0	0	0	1	0	1	0	0x0A	4DP
			1	0	0	1	0	0	1	0x49	8DP
			1	0	1	1	0	0	1	0x59	16DP
	13	0	0	0	0	0	0	0	1	0x01	Sub channel = 16 bits
	16	0	0	0	0	0	0	0	0	0x00	2DP signal loading
		0	1	0	0	1	0	0	0	0x48	4DP signal loading
		0	1	0	1	0	0	0	1	0x51	8DP signal loading
		1	0	0	1	1	0	0	1	0x99	16DP signal loading
	230	0	0	0	1	0	0	1	1	0x13	CAMM2 module height (34.0 mm)
	231	0	0	0	0	0	0	0	1	0x01	Thickness: Back (0-1 mm), Top (1-2 mm)
	232	0	0	0	0	0	1	0	0	0x04	Raw card "E0"
	233 ¹	1	0	0	0	0	0	0	1	0x81	XT, no heat spreader, 1-row
	234	0	0	0	0	0	0	0	0	0x00	2DP – 1 package rank
				0	0	1				0x08	4DP – 2 package rank
				0	0	1				0x08	8DP – 2 package rank
				0	1	1				0x18	16DP – 4 package rank
	235	0	1	1	0	0	0	0	1	0x61	8 sub-channels, no ECC, 16-bit bus per channel

NOTE 1 CAMM2 vendor has option to update/set these bits.

19 Cross Section Recommendations

PCBs should contain solid ground plane and power plane layers as far as possible. CAMM2 vendors to confirm stack from supplier to meet impedance targets.

The PCB edge connector contacts shall be gold plated.

Any exceptions to design rules have been identified in the front of this Annex.

Table 20 — PCB Fabrication Table – E0

Layer	Layer Description	Single-ended Impedances		Differential Impedances		Copper (μm)	Dielectric Thickness (μm)
		Trace Width (mm)	Impedance (ohm)	Trace Width / Spacing (mm / mm)	Impedance (ohm)		
1	Signal	0.140	40±10%			0.3 + Plating (41)	
	Signal	0.175	35±10%				
	Dielectric						50
2	GND					32	
	Dielectric						60
3	Signal	0.085	40±10%	0.090 / 0.100	75±15%	35	
	Vddq/Vin_bulk/Vdd2			0.115 / 0.100	65±15%		
	Dielectric						60
4	GND					30	
	Dielectric						60
5	Address / Vdd1	0.135	40±10%			30	
	Dielectric						405
6	Vdd2 / GND					30	
	Dielectric						60
7	GND					30	
	Dielectric						60
8	Signal / GND	0.085	40±10%	0.090 / 0.100	75±15%	35	
	Vddq/Vin_bulk/Vdd2			0.115 / 0.100	65±15%		
							60
9	GND / Vin_bulk					32	
							50
10	Signal	0.140	40±10%			0.3 + Plating (41)	
	Signal	0.175	35±10%				
NOTE 1 The recommended construction and impedance can be found in the PCB Fabrication Table. The values in the table were used in the simulations during development and in the initial CAMM2's used to verify operation. Deviations should be kept to a minimum.							



Standard Improvement Form**JEDEC Standard No. JESD318-F0-RCE**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

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